REMARKS

Applicants respectfully request reconsideration of this application in light of this submission. Claims 1 to 31 are pending. Of these claims, claims 1, 11, 20, and 29 are independent.

In the Office Action mailed May 18, 2007, the Examiner rejected the independent claims (1, 11, 20, and 29) as unpatenably obvious over U.S. Patent No. 5,905,874 ("Johnson") in view of U.S. Patent No. 7,065,762 ("Duda"). (The remaining claims were also rejected as obvious over Johnson and Duda further in view of other references; however, they will not be addressed in detail at this time since as will be shown, Johnson and Duda do not render the independent claims unpatentable and thus the remaining claims are also not unpatentable at least due to reliance on Johnson and Duda as urged by the Examiner.)

Applicants maintain that Johnson and Duda, individually or in combination, fail to teach, disclose, or suggest each and every element of the claims.

Johnson discloses an I/O device, (NIC) that is directed to improving data transfer latency. But it does not teach using interrupts in any way to achieve this objective. Rather, it teaches initiating writing network received data into the computer's memory (from the interface buffer) without waiting for the data to be completely loaded into the buffer. (See Johnson at col. 3, ll. 42-58). As recognized by the Examiner, nowhere does it teach moderating interrupts to a processor based on a characterization that received data fragments (packets)

are latency sensitive. As discussed below, Duda does not provide this missing feature and for this reason alone, the two references cannot render Applicant's claims unpatentable because alone or in combination, they do not teach every claimed element.

In addition, however, Johnson actually teaches away from its being modified in this way. It states that memory mapped schemes, which use interrupts to invoke the host processor to service network interface data transfer tasks, are less desirable than direct memory access (DMA) methods because they involve inefficiency and require valuable host processor resources. (See Johnson at col. 7, l. 60 to col. 8, l. 2; col. 2, ll. 40-52). In other words, Johnson counsels against using interrupts to involve the processor in servicing a NIC data transfer task. Thus, based on these teachings, one would certainly not look for or consider any kind of an interrupt based solution for improving latency or otherwise modifying Johnson in this way. Therefore, the references may not be combined (or Johnson be modified) as is urged by the Examiner.

Even if Duda could be combined with Johnson, however, the references would still fail to teach or suggest moderating processor interrupts based on a characterization that a data fragment is latency sensitive. Duda does disclose a system that is concerned with reducing latency, e.g., to reduce the processing of data packets in a switch in a computer. However, to do this, it teaches that an incoming data packet is to be placed in an appropriate (e.g., higher priority) queue based on whether it has latency sensitive data. (See, e.g., Duda at col. 5,

ll. 14-20). This may sound close to Applicant's feature, but apart from characterizing whether the packet has latency sensitive data, it doesn't teach the feature. The different queues don't act to moderate interrupts (e.g., control when they are released) to the processor. Instead, higher priority queues simply get more time to be serviced by the processor when their "turn" arises. Duda teaches that its preemptive scheduling controls when timer interrupts are entered, but these are initiated from within the processor and used to control how long a task is serviced. Duda does not teach moderating processor interrupts (e.g., when they are invoked by an I/O device) based on the latency sensitivity characterization of a packet by the I/O device. Thus, even if the references could be combined (which they cannot), they still fail to teach each and every claimed element. Accordingly, the rejections should be withdrawn.

Conclusion

Applicants respectfully submit that the claims overcome the cited prior art, and are in condition for allowance. Therefore, allowance at an early date is respectfully requested.

The Examiner is invited to initiate an interview with the undersigned by calling 512/238-7253 if the Examiner believes that such an interview will advance prosecution of this application.

Respectfully submitted,

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/Erik Nordstrom, Reg. No. 39,792/

Erik R. Nordstrom
Registration No. 39,792